



## CTL147NS10-T52

### N-Channel Enhancement MOSFET

#### Features

- Drain-Source Breakdown Voltage  $V_{DSS}$  100V
- Drain-Source On-Resistance  
 $R_{DS(ON)}$  80m $\Omega$ , at  $V_{GS} = 10V$ ,  $I_D = 8A$
- Continuous Drain Current at  $T_C = 25^\circ C$   $I_D = 14.7A$
- Advanced high cell density Trench Technology
- RoHS Compliance & Halogen Free

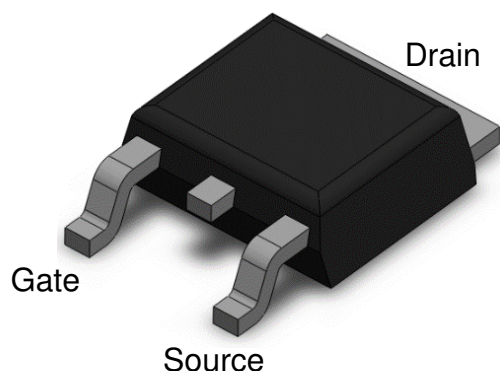
#### Applications

- DC/DC Converter
- Load Switch
- LCD Display inverter

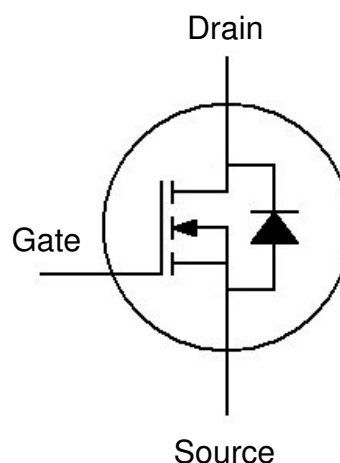
#### Description

The CTL147NS10-T52 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application.

#### Package Outline



#### Schematic





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### Absolute Maximum Rating at 25°C

| Symbol           | Parameters                                     | Test Conditions | Min | Note |
|------------------|--|-----------------|-----|------|
| V <sub>DS</sub>  | Drain-Source Voltage                           | 100             | V   |      |
| V <sub>GS</sub>  | Gate-Source Voltage                            | ±20             | V   |      |
| I <sub>D</sub>   | Continuous Drain Current @T <sub>C</sub> =25°C | 14.7            | A   | 1    |
| I <sub>DM</sub>  | Pulsed Drain Current                           | 59              | A   | 1    |
| P <sub>D</sub>   | Total Power Dissipation @T <sub>C</sub> =25°C  | 34.7            | W   | 2    |
| T <sub>STG</sub> | Storage Temperature Range                      | -55 to 150      | °C  |      |
| T <sub>J</sub>   | Operating Junction Temperature Range           | -55 to 150      | °C  |      |

### Thermal Characteristics

| Symbol           | Parameters                          | Test Conditions | Min | Typ | Max | Units | Notes |
|------------------|-------------------------------------|-----------------|-----|-----|-----|-------|-------|
| R <sub>θJC</sub> | Thermal Resistance<br>Junction-Case |                 | --  | --  | 3.6 | °C /W | 1,4   |



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### Electrical Characteristics $T_A = 25^\circ\text{C}$ (unless otherwise specified)

#### Static Characteristics

| Symbol     | Parameters                     | Test Conditions                 | Min | Typ | Max       | Units   | Notes |
|------------|--------------------------------|---------------------------------|-----|-----|-----------|---------|-------|
| $B_{VDSS}$ | Drain-Source Breakdown Voltage | $V_{GS} = 0V, I_D = 250\mu A$   | 100 | -   | -         | V       |       |
| $I_{DSS}$  | Drain-Source Leakage Current   | $V_{DS} = 80V, V_{GS} = 0V$     | -   | -   | 1         | $\mu A$ |       |
| $I_{GSS}$  | Gate-Source Leakage Current    | $V_{GS} = \pm 20V, V_{DS} = 0V$ | -   | -   | $\pm 100$ | nA      |       |

#### On Characteristics

| Symbol       | Parameters                    | Test Conditions                   | Min | Typ | Max | Units      | Notes |
|--------------|-------------------------------|-----------------------------------|-----|-----|-----|------------|-------|
| $R_{DS(ON)}$ | Drain-Source On-Resistance    | $V_{GS} = 10V, I_D = 8A$          | -   | 80  | 100 | m $\Omega$ | 3     |
| $V_{GS(th)}$ | Gate-Source Threshold Voltage | $V_{GS} = V_{DS}, I_D = 250\mu A$ | 1.0 | -   | 3.0 | V          | 3     |

#### Dynamic Characteristics

| Symbol    | Parameters                   | Test Conditions | Min | Typ | Max | Units | Notes |
|-----------|------------------------------|-----------------|-----|-----|-----|-------|-------|
| $C_{ISS}$ | Input Capacitance            | $V_{GS} = 0V,$  | -   | 890 | -   | pF    |       |
| $C_{OSS}$ | Output Capacitance           | $V_{DS} = 15V$  | -   | 58  | -   |       |       |
| $C_{RSS}$ | Reverse Transfer Capacitance | $f = 1MHz$      | -   | 23  | -   |       |       |

#### Switching Characteristics

| Symbol       | Parameters                 | Test Conditions  | Min | Typ | Max | Units | Notes |
|--------------|----------------------------|--|-----|-----|-----|-------|-------|
| $T_{D(ON)}$  | Turn-On Delay Time         | $V_{DS} = 50V, R_G = 1\Omega$<br>$V_{GS} = 10V, R_L = 5\Omega$ | -   | 14  | -   | ns    |       |
| $T_R$        | Rise Time                  |  | -   | 33  | -   |       |       |
| $T_{D(OFF)}$ | Turn-Off Delay Time        |  | -   | 39  | -   |       |       |
| $T_F$        | Fall Time                  |  | -   | 5   | -   |       |       |
| $Q_G$        | Total Gate Charge          | $V_{DS} = 80V,$<br>$V_{GS} = 4.5V,$<br>$I_D = 10A$             | -   | 13  | -   | nC    |       |
| $Q_{GS}$     | Gate-Source Charge         |  | -   | 4.6 | -   |       |       |
| $Q_{GD}$     | Gate-Drain (Miller) Charge |  | -   | 7.6 | -   |       |       |



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### Drain-Source Diode Characteristics

| Symbol   | Parameters                    | Test Conditions            | Min | Typ | Max | Units | Notes |
|----------|-------------------------------|----------------------------|-----|-----|-----|-------|-------|
| $V_{SD}$ | Body Diode Forward Voltage    | $V_{GS} = 0V, I_{SD} = 1A$ | -   | 0.9 | 1.2 | V     | 1     |
| $I_{SD}$ | Body Diode Continuous Current |                            | -   | -   | 1   | A     | 1     |

Note:

1. The power dissipation is limited by 150°C junction temperature.
2. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
3. Thermal Resistance follow JESD51-3.



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### Typical Characteristic Curves

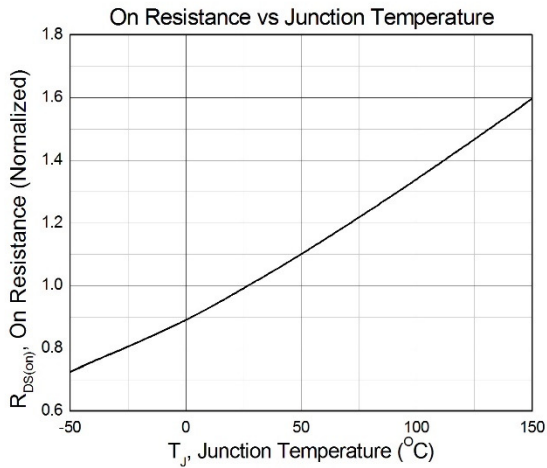


Figure 1

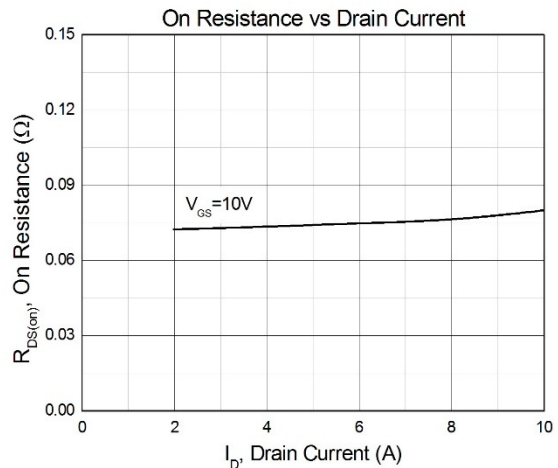


Figure 2

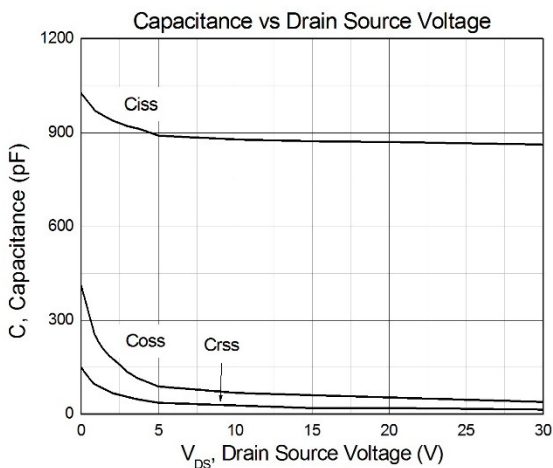


Figure 3

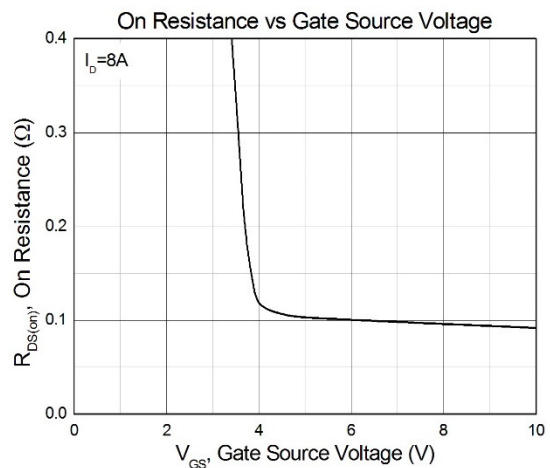


Figure 4

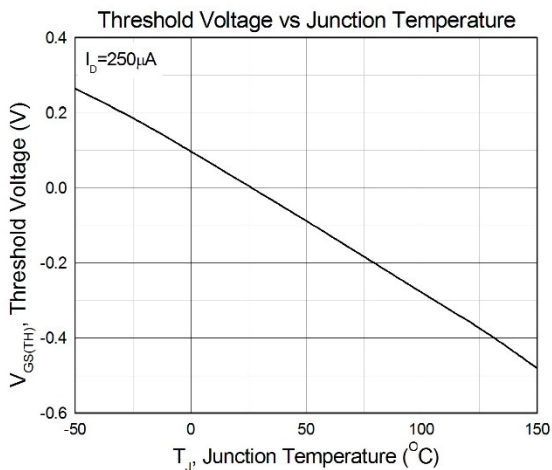


Figure 5

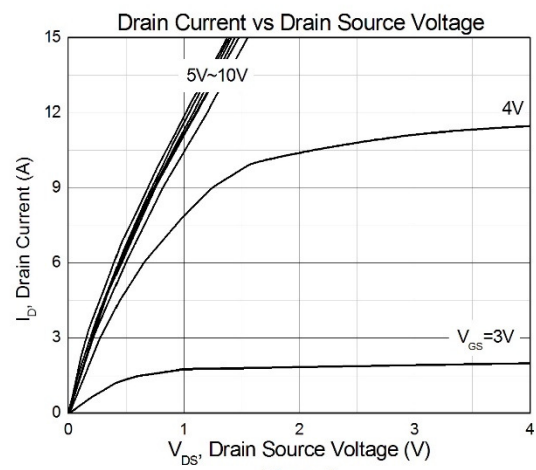


Figure 6



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## N-Channel Enhancement MOSFET

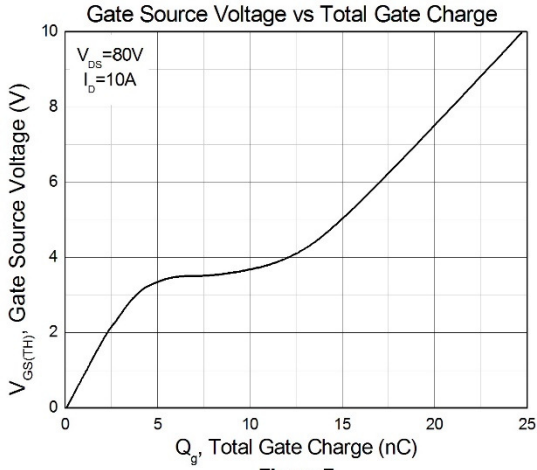


Figure 7

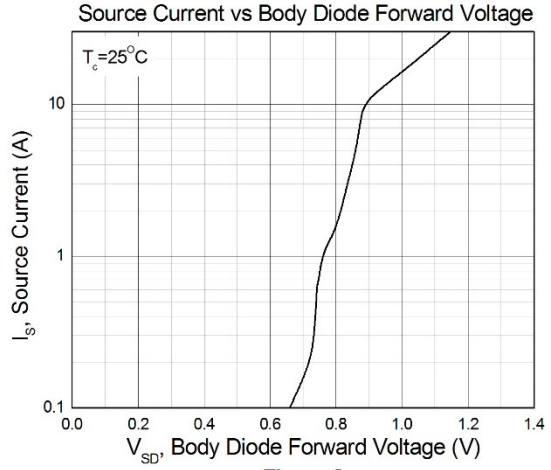


Figure 8



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## N-Channel Enhancement MOSFET

### Test Circuits & Waveforms

Figure 9: Gate Charge Test Circuit

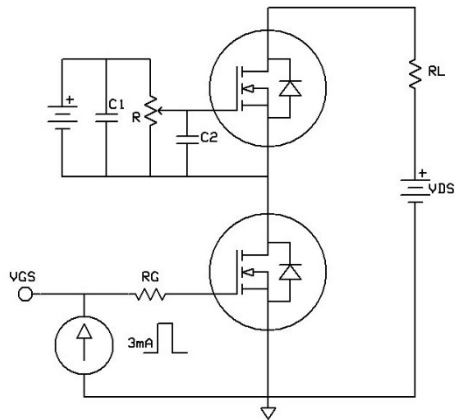


Figure 10: Gate Charge Waveform

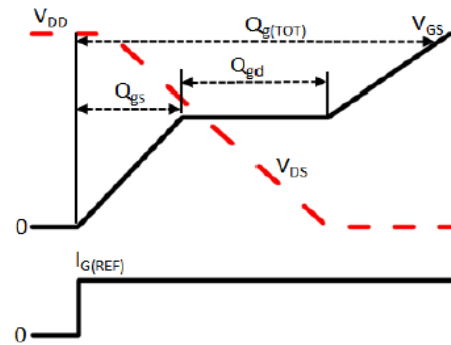


Figure 11: Switching Time Test Circuit

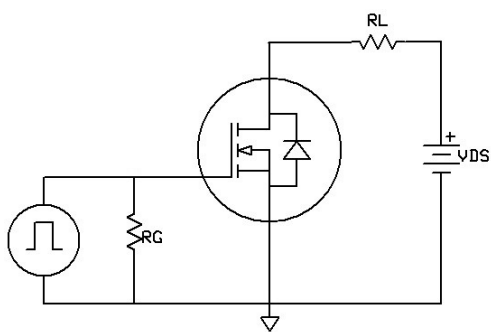
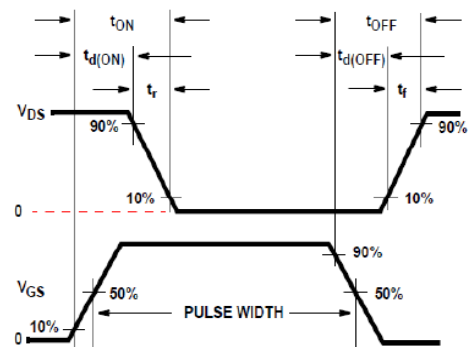


Figure 12: Switching Time Waveform

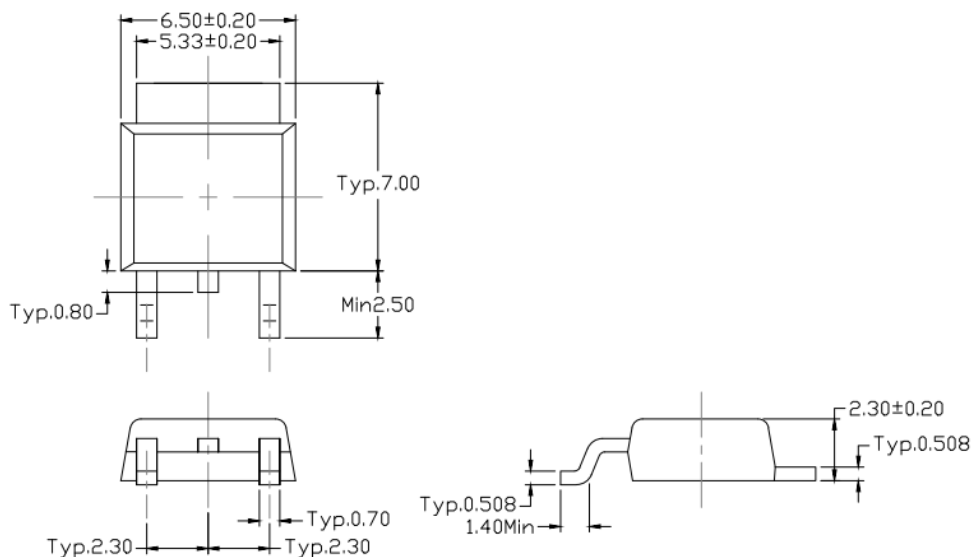




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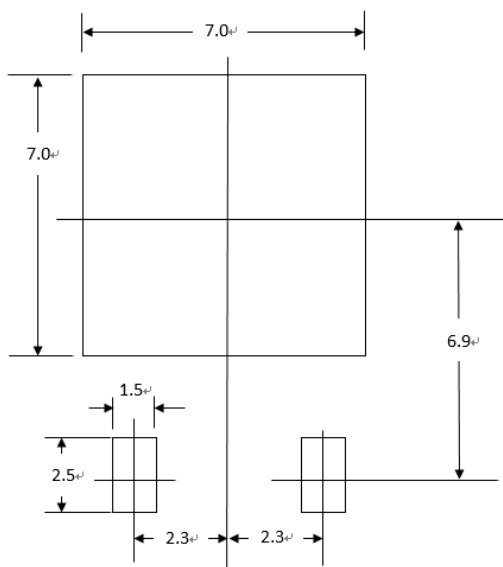
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### Package Dimension (TO-252)



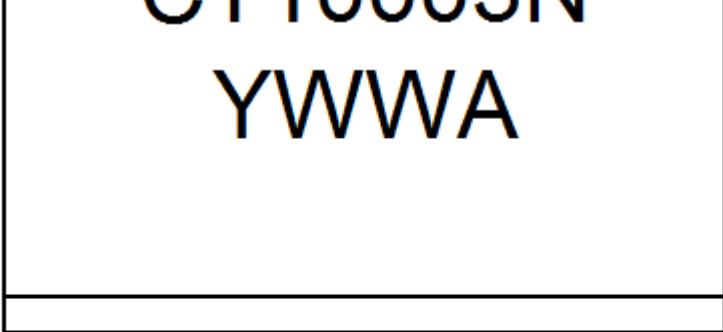
Dimensions in mm unless otherwise stated

### Recommended pad layout for surface mount leadform

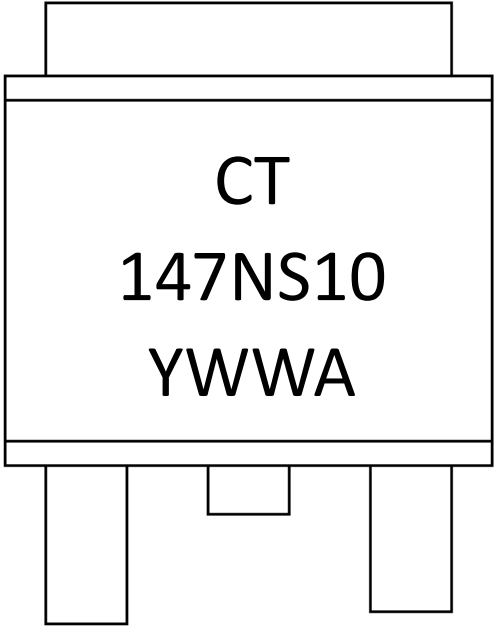


Dimensions in mm unless otherwise stated





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**Channel Enhancement MOSFET**



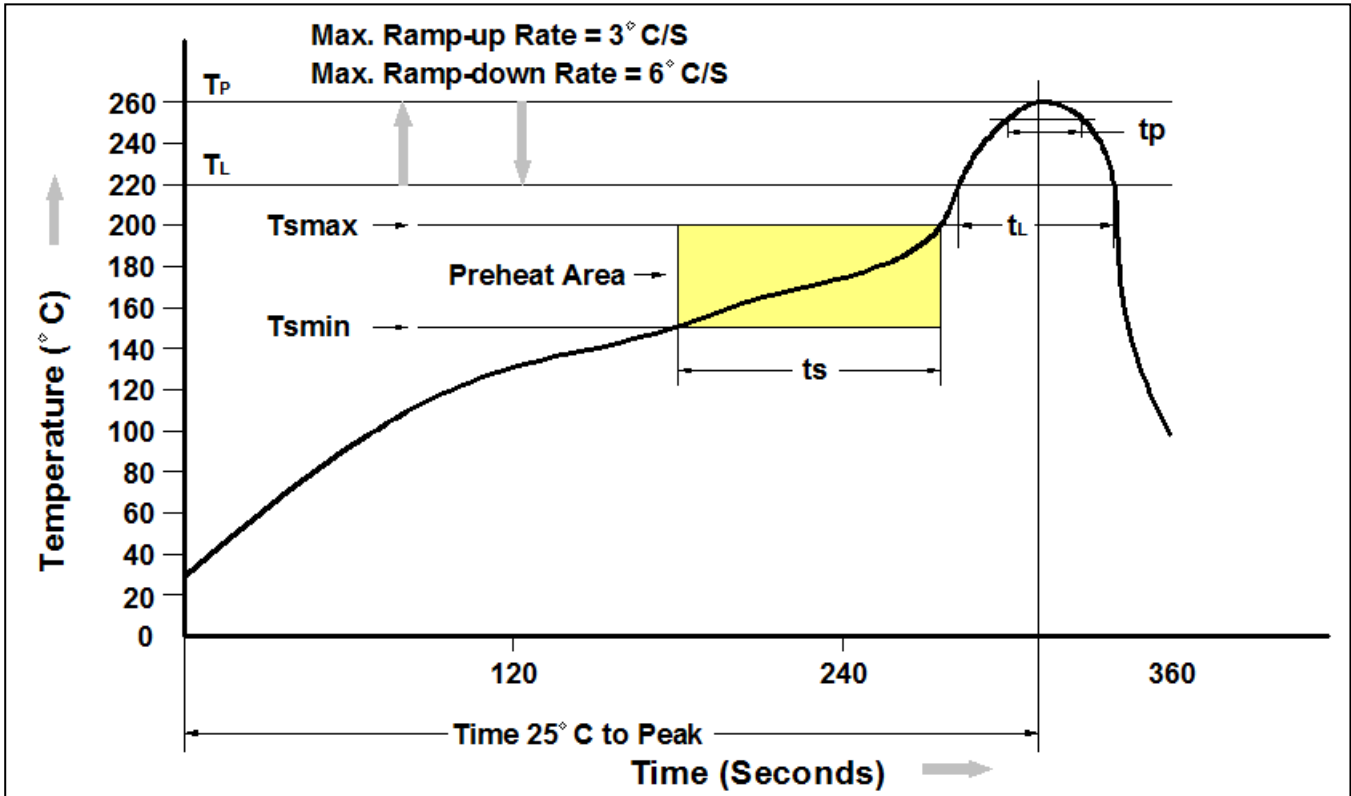
CT : Denotes "CT M"  
 147NS10 : Device Number  
 Y : Fiscal Year  
 WW : Work Week  
 A : Production Code

**Ordering Information**

| <b>Part Number</b> | <b>Description</b> | <b>Quantity</b> |
|--------------------|--------------------|-----------------|
| CTL147NS10-T52     | TO-252 Reel        | 2500 pcs        |



Reflow Profile



| Profile Feature   | Pb-Free Assembly Profile |
|---|--------------------------|
| Temperature Min. (T <sub>smin</sub> )                                 | 150 °C                   |
| Temperature Max. (T <sub>smax</sub> )                                 | 200 °C                   |
| Time (t <sub>s</sub> ) from (T <sub>smin</sub> to T <sub>smax</sub> ) | 60-120 seconds           |
| Ramp-up Rate (t <sub>L</sub> to t <sub>P</sub> )                      | 3°C/second max.          |
| Liquidous Temperature (T <sub>L</sub> )                               | 217 °C                   |
| Time (t <sub>L</sub> ) Maintained Above (T <sub>L</sub> )             | 60 – 150 seconds         |
| Peak Body Package Temperature   | 260 °C +0 °C / -5 °C     |
| Time (t <sub>P</sub> ) within 5 °C of 260 °C                          | 30 seconds               |
| Ramp-down Rate (T <sub>P</sub> to T <sub>L</sub> )                    | 6°C/second max           |
| Time 25 °C to Peak Temperature  | 8 minutes max.           |



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