



CTH6402NS-T52

N-Channel Enhancement MOSFET

Features

- Drain-Source Breakdown Voltage V_{DSS} 25V
- Drain-Source On-Resistance
 $R_{DS(ON)}$ 4m Ω , at $V_{GS}= 10$, $I_D= 30A$
 $R_{DS(ON)}$ 8m Ω , at $V_{GS}= 5$, $I_D= 15A$
- Continuous Drain Current at $T_C=25^\circ C$ $I_D =64A$
- Advanced high cell density Trench Technology
- RoHS Compliance & Halogen Free

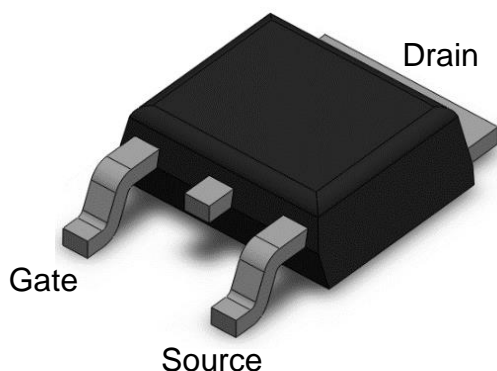
Description

The CTH6402NS –T52 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application.

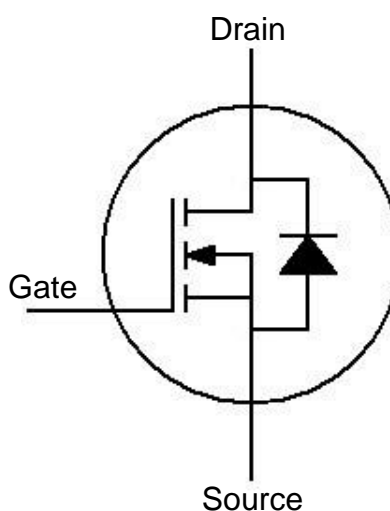
Applications

- DC/DC Converter
- Load Switch
- LCD Display inverter
- IPC

Package Outline



Schematic





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N-Channel Enhancement MOSFET

Absolute Maximum Rating at 25°C

Symbol	Parameters	Test Conditions	Min	Notes
V _{DS}	Drain-Source Voltage	25	V	
V _{GS}	Gate-Source Voltage	±20	V	
I _D	Continuous Drain Current @T _C =25°C	64	A	1
I _{DM}	Pulsed Drain Current	100	A	1
P _D	Total Power Dissipation @T _C =25°C	41	W	2
EAS	Pulsed Avalanche Rating	100	mJ	
T _{STG}	Storage Temperature Range	-55 to 150	°C	
T _J	Operating Junction Temperature Range	-55 to 150	°C	

Thermal Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
R _{θJA}	Thermal Resistance Junction-Ambient		--	--	3.0	°C/W	1,4



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Electrical Characteristics $T_A = 25^\circ\text{C}$ (unless otherwise specified)

Static Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$B_{V_{DS}}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	25	-	-	V	
I_{DSS}	Drain-Source Leakage Current	$V_{DS} = 25V, V_{GS} = 0V$	-	-	1	μA	
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	± 100	nA	

On Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$R_{DS(ON)}$	Drain-Source On-Resistance	$V_{GS} = 10V, I_D = 30A$	-	4.0	6.0	m Ω	3
		$V_{GS} = 5V, I_D = 15A$	-	8.0	13.0	m Ω	3
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu A$	1.0	-	3.0	V	3

Dynamic Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
C_{ISS}	Input Capacitance	$V_{GS} = 0V,$ $V_{DS} = 15V$ $f = 1MHz$	-	1605	-	pF	
C_{OSS}	Output Capacitance		-	335	-		
C_{RSS}	Reverse Transfer Capacitance		-	105	-		

Switching Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$T_{D(ON)}$	Turn-On Delay Time	$V_{DS} = 15V,$ $V_{GS} = 10V,$ $R_G = 3\Omega,$ $I_D = 1A$	-	17.5	-	ns	
T_R	Rise Time		-	15.2	-		
$T_{D(OFF)}$	Turn-Off Delay Time		-	58.5	-		
T_F	Fall Time		-	6.2	-		
Q_G	Total Gate Charge	$V_{DS} = 15V,$ $V_{GS} = 4.5V,$ $I_D = 25A$	-	19.6	-	nC	
Q_{GS}	Gate-Source Charge		-	8.2	-		
Q_{GD}	Gate-Drain (Miller) Charge		-	11.3	-		



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Drain-Source Diode Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
V_{SD}	Body Diode Forward Voltage	$V_{GS} = 0V, I_{SD} = 20A$	-	0.85	1.2	V	1
I_{SD}	Body Diode Continuous Current		-	-	64	A	1

Note:

1. The power dissipation is limited by 150°C junction temperature.
2. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. Thermal Resistance follow JESD51-3.



Typical Characteristic Curves

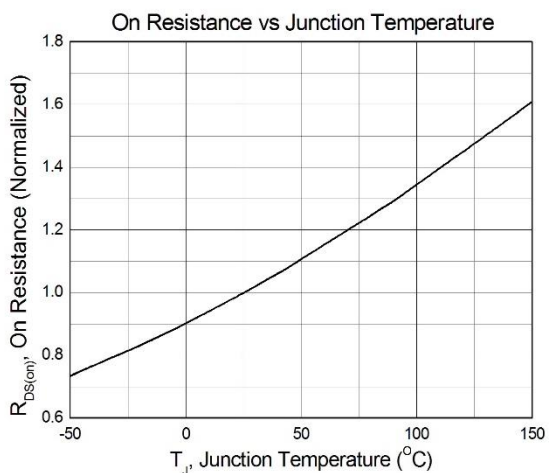


Figure 1

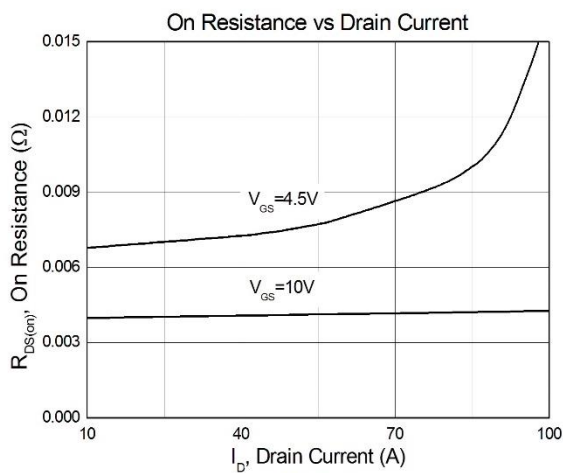


Figure 2

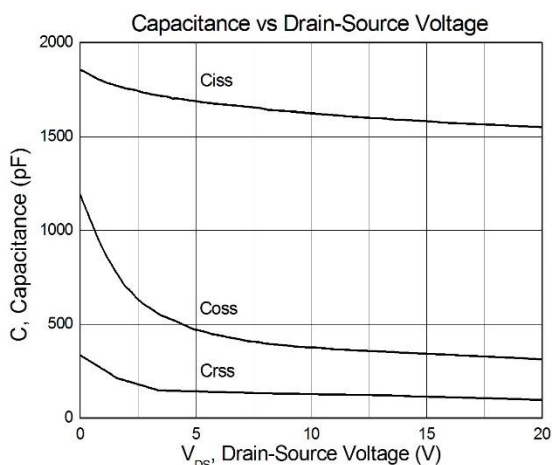


Figure 3

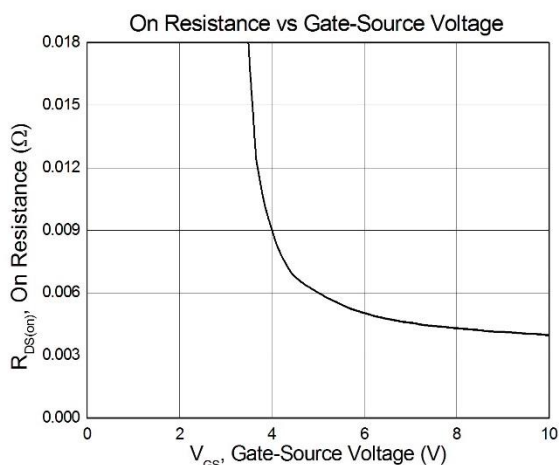


Figure 4

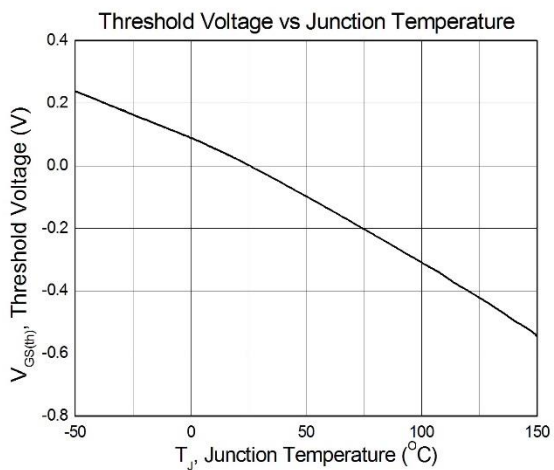


Figure 5

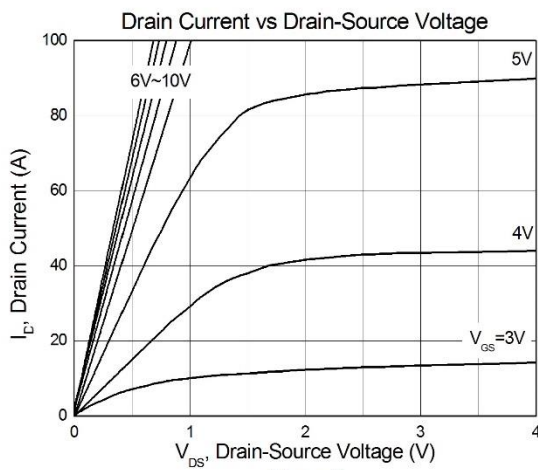


Figure 6

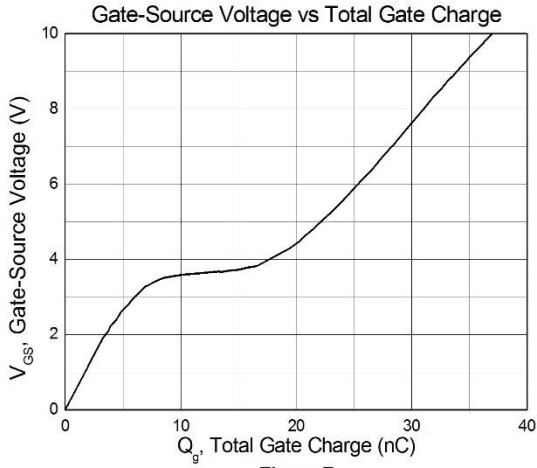


Figure 7

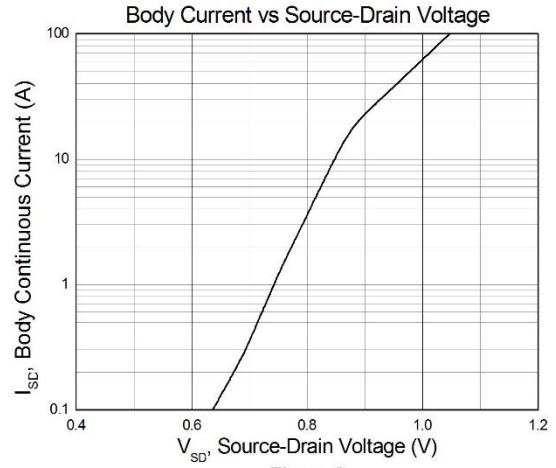


Figure 8



Test Circuits & Waveforms

Figure 9: Gate Charge Test Circuit

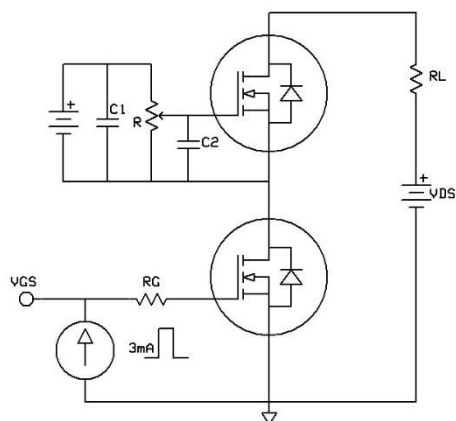


Figure 10: Gate Charge Waveform

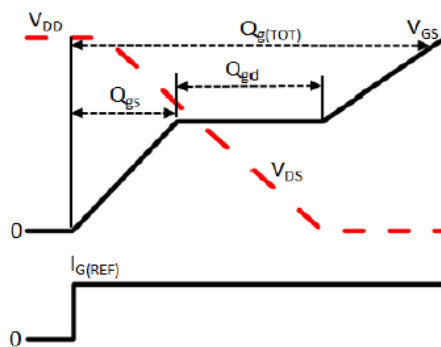


Figure 11: Switching Time Test Circuit

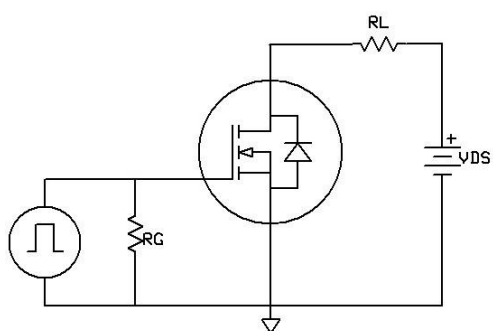
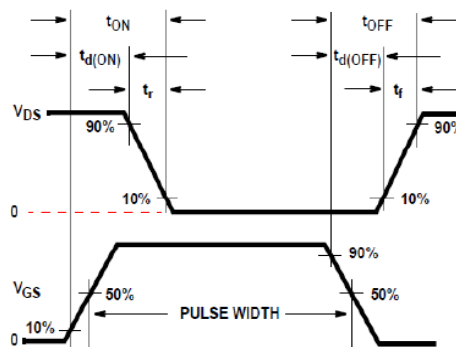
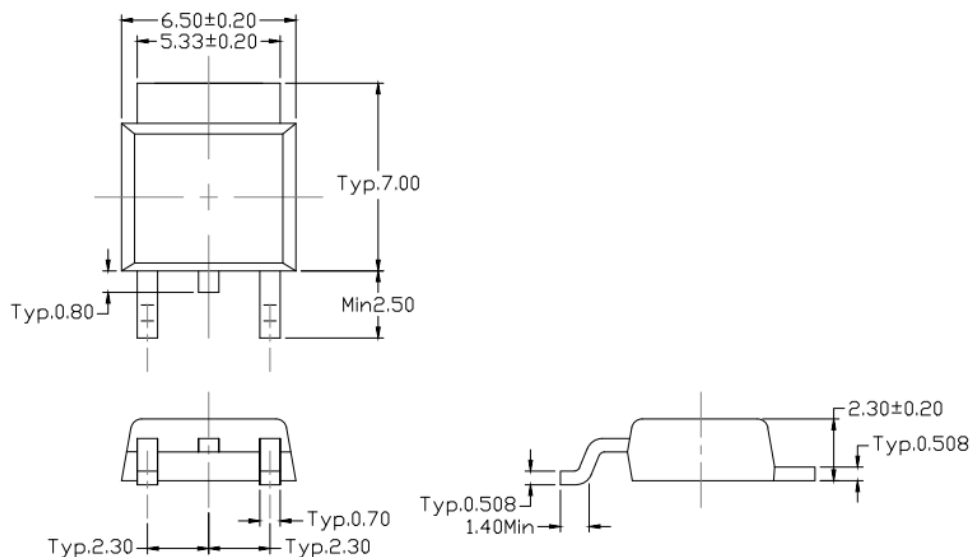


Figure 12: Switching Time Waveform



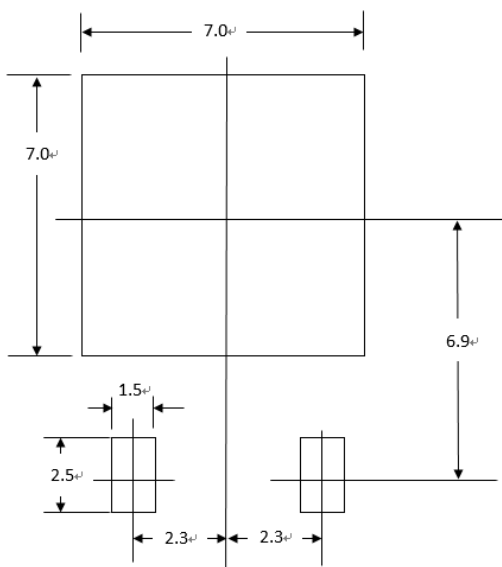


Package Dimension (TO-252)



Dimensions in mm unless otherwise stated

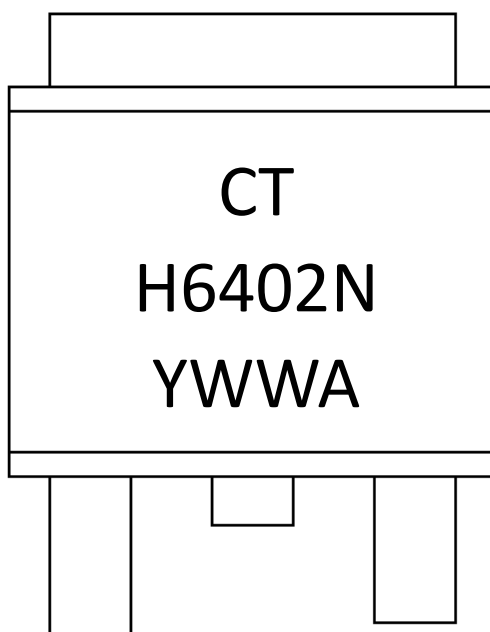
Recommended pad layout for surface mount leadform



Dimensions in mm unless otherwise stated



Marking Information



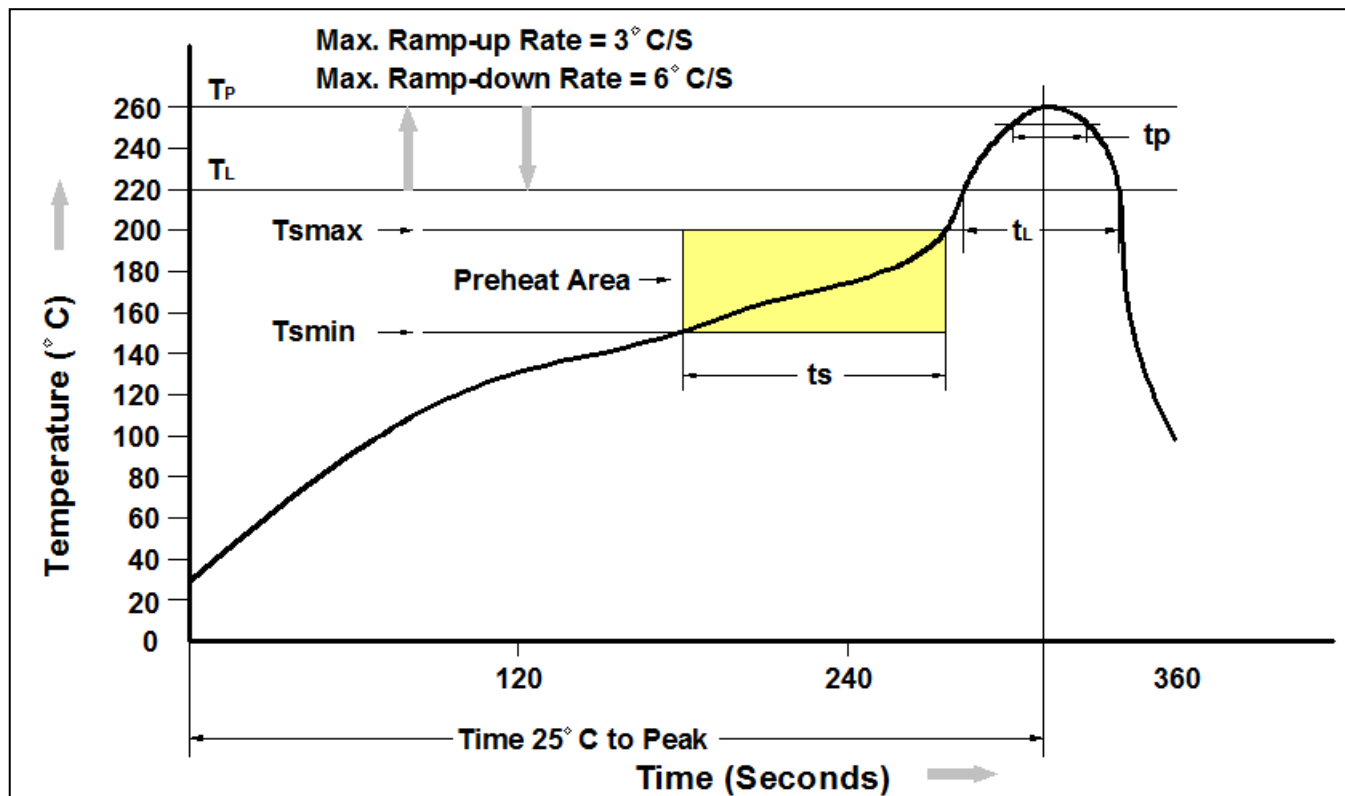
- CT : Denotes “ CT Micro”
- H6402N : Device Number
- Y : Fiscal Year
- WW : Work Week
- A : Production Code

Ordering Information

Part Number	Description	Quantity
CTH6402NS-T52	TO-252 Reel	2500 pcs



Reflow Profile



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (Tsmín)	150°C
Temperature Max. (Tsmáx)	200°C
Time (ts) from (Tsmín to Tsmáx)	60-120 seconds
Ramp-up Rate (tL to tP)	3°C/second max.
Liquidous Temperature (TL)	217°C
Time (tL) Maintained Above (TL)	60 – 150 seconds
Peak Body Package Temperature	260°C +0°C / -5°C
Time (tP) within 5°C of 260°C	30 seconds
Ramp-down Rate (TP to TL)	6°C/second max
Time 25°C to Peak Temperature	8 minutes max.



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