



CTH3904NS-T52

N-Channel Enhancement MOSFET

Features

- Drain-Source Breakdown Voltage V_{DSS} 40V
- Drain-Source On-Resistance
 $R_{DS(ON)}$ 9m Ω , at $V_{GS}= 10V$, $I_D= 15A$
 $R_{DS(ON)}$ 13m Ω , at $V_{GS}= 4.5V$, $I_D= 13A$
- Continuous Drain Current at $T_C=25^\circ C$ I_D 39A
- Advanced high cell density Trench Technology
- RoHS Compliance & Halogen Free

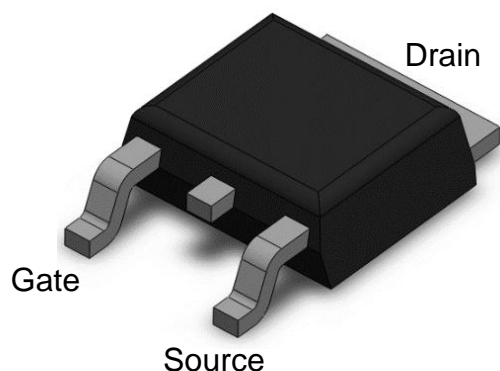
Description

The CTH3904NS-T52 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application.

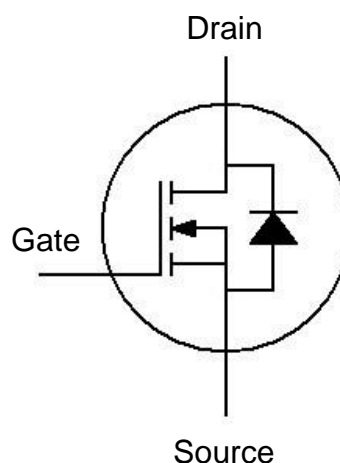
Applications

- Power Management
- DC/DC Converter
- LCD TV & Monitor Display inverter
- CCFL inverter

Package Outline



Schematic





CTH3904NS-T52

N-Channel Enhancement MOSFET

Absolute Maximum Rating at 25°C

Symbol	Parameters	Test Conditions	Min	Note
V _{DS}	Drain-Source Voltage	40	V	
V _{GS}	Gate-Source Voltage	±20	V	
I _D	Continuous Drain Current @T _c =25°C	39	A	1
I _{DM}	Pulsed Drain Current	156	A	1
P _D	Total Power Dissipation @T _c =25°C	29	W	2
T _{STG}	Storage Temperature Range	-55 to 150	°C	
T _J	Operating Junction Temperature Range	-55 to 150	°C	

Thermal Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
R _{θJC}	Thermal Resistance Junction-Case		--	--	3.9	°C/W	1,4



N-Channel Enhancement MOSFET

Electrical Characteristics $T_A = 25^\circ\text{C}$ (unless otherwise specified)

Static Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$B_{V_{DS}}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	40	-	-	V	
I_{DSS}	Drain-Source Leakage Current	$V_{DS} = 40V, V_{GS} = 0V$	-	-	1	μA	
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	± 100	nA	

On Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$R_{DS(ON)}$	Drain-Source On-Resistance	$V_{GS} = 10V, I_D = 15A$	-	9	12	$m\Omega$	3
		$V_{GS} = 4.5V, I_D = 13A$	-	13	17	$m\Omega$	
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu A$	1.0	-	3.0	V	3

Dynamic Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
C_{ISS}	Input Capacitance	$V_{GS} = 0V,$ $V_{DS} = 20V$ $f = 1MHz$	-	1250	1500	pF	
C_{OSS}	Output Capacitance		-	170	-		
C_{RSS}	Reverse Transfer Capacitance		-	60	-		

Switching Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$T_{D(ON)}$	Turn-On Delay Time	$V_{DS} = 20V,$ $V_{GS} = 10V,$ $R_G = 6\Omega$ $I_D = 1A$	-	16	20	ns	
T_R	Rise Time		-	13	17		
$T_{D(OFF)}$	Turn-Off Delay Time		-	60	75		
T_F	Fall Time		-	7	10		
Q_G	Total Gate Charge	$V_{DS} = 20V,$ $V_{GS} = 10V,$ $I_D = 15A$	-	16	18	nC	
Q_{GS}	Gate-Source Charge		-	6.5	-		
Q_{GD}	Gate-Drain (Miller) Charge		-	8.3	-		



CTH3904NS-T52

N-Channel Enhancement MOSFET

Drain-Source Diode Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
V_{SD}	Body Diode Forward Voltage	$V_{GS} = 0V, I_{SD} = 1.0A$	-	0.8	1.2	V	1
I_{SD}	Body Diode Continuous Current		-	-	1.0	A	1

Note:

1. The power dissipation is limited by 150°C junction temperature.
2. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. Thermal Resistance follow JESD51-3.



Typical Characteristic Curves

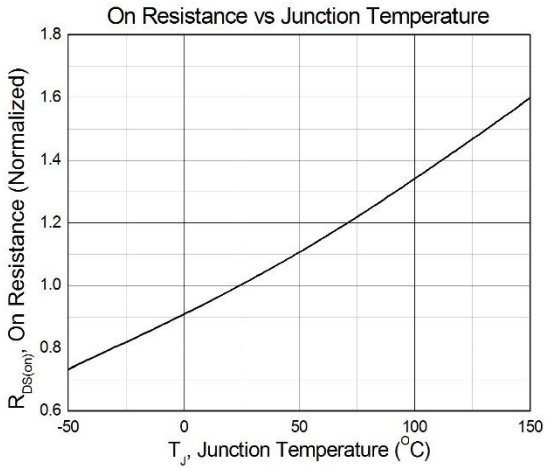


Figure 1

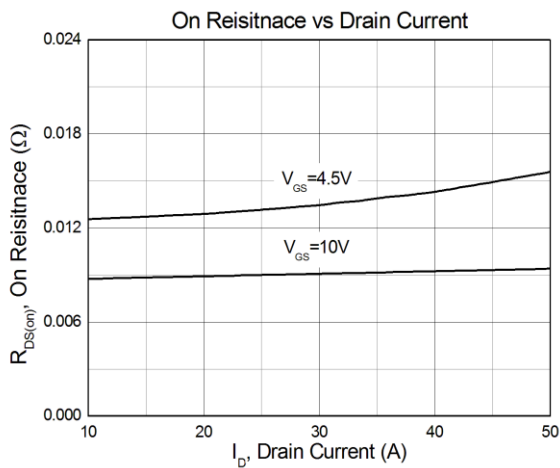


Figure 2

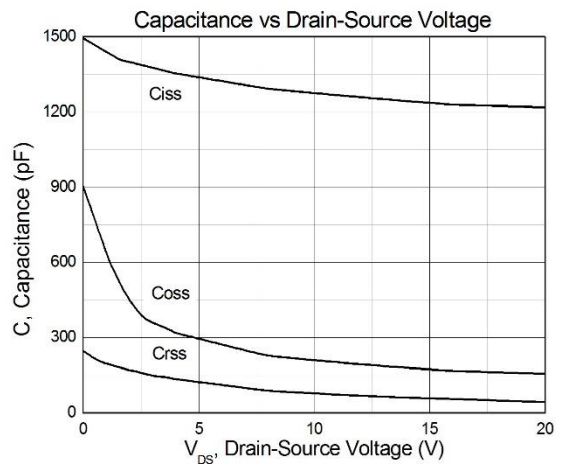


Figure 3

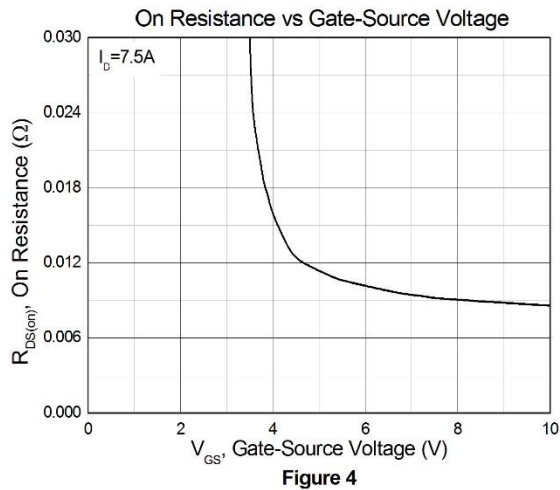


Figure 4

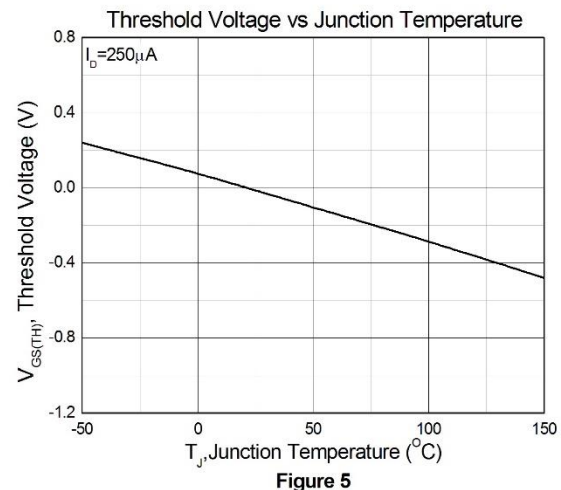
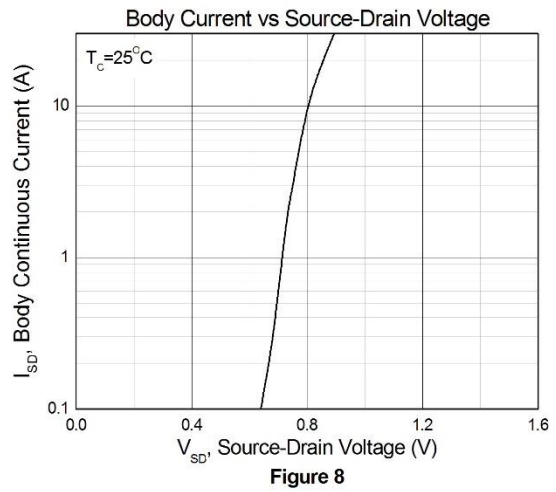
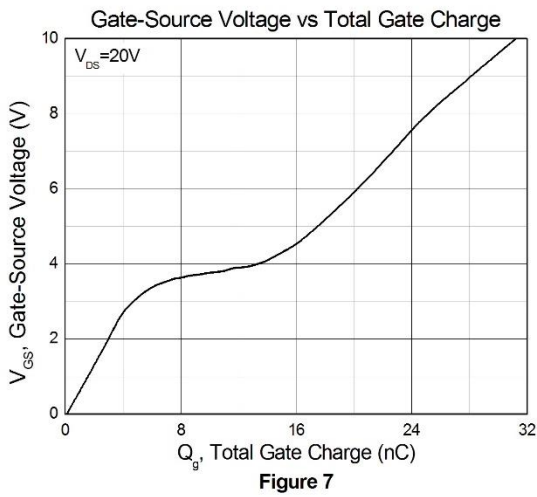
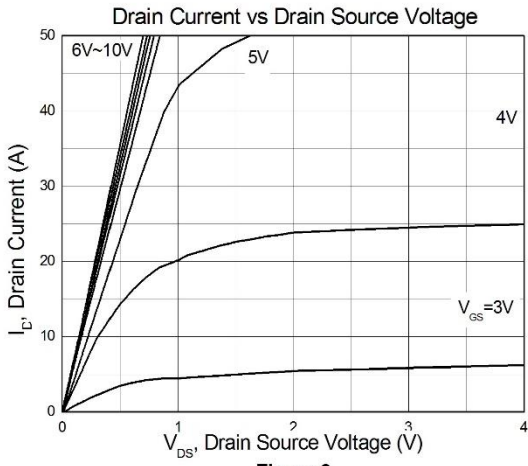


Figure 5





Test Circuits & Waveforms

Figure 9: Gate Charge Test Circuit

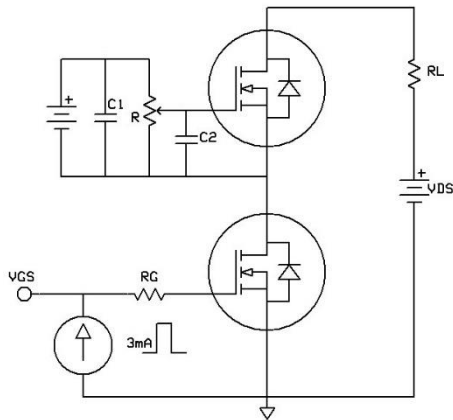


Figure 10: Gate Charge Waveform

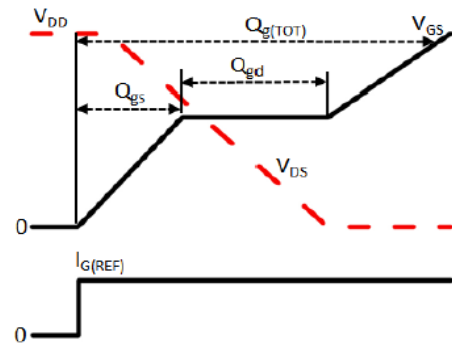


Figure 11: Switching Time Test Circuit

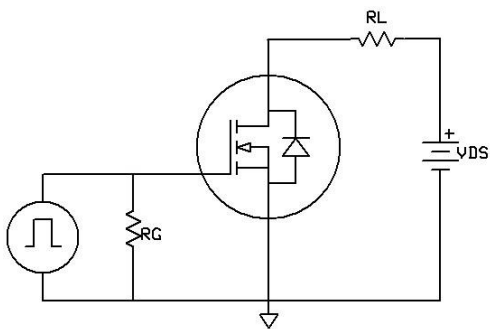
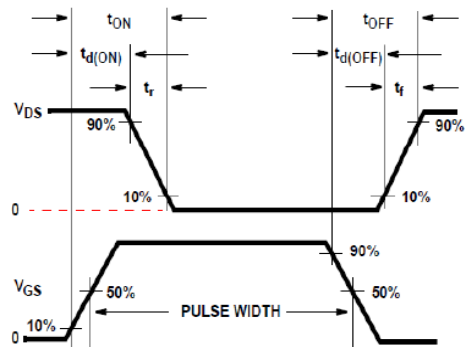
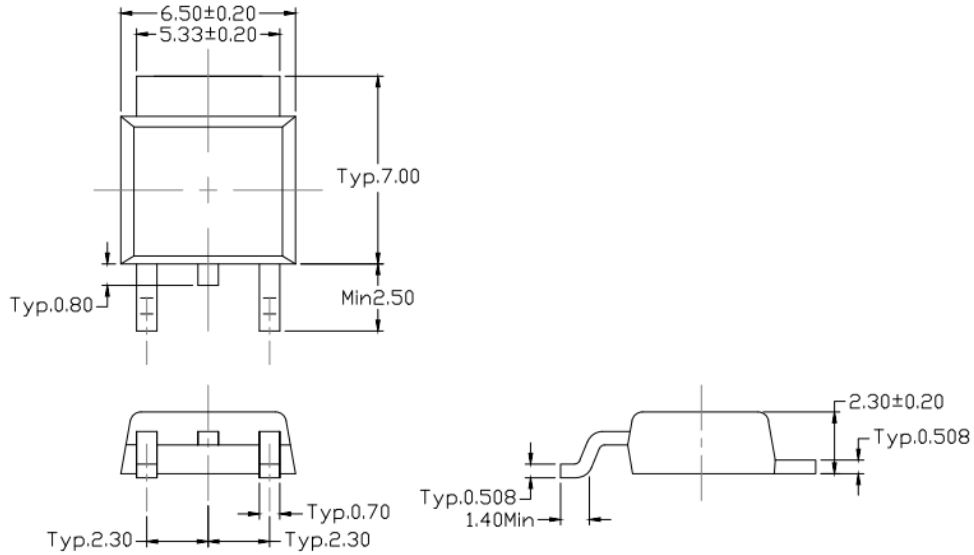


Figure 12: Switching Time Waveform



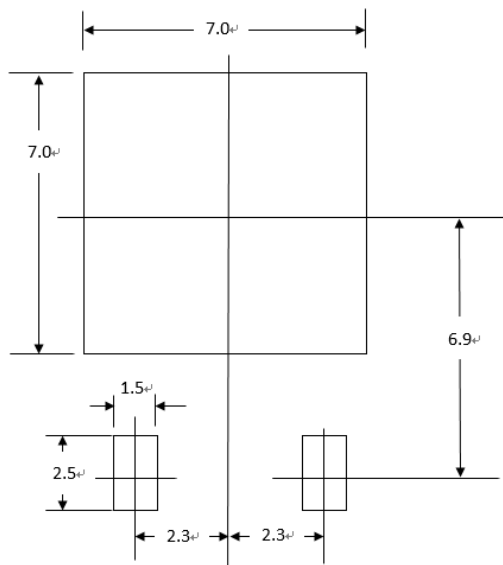


Package Dimension (TO-252)



Dimensions in mm unless otherwise stated

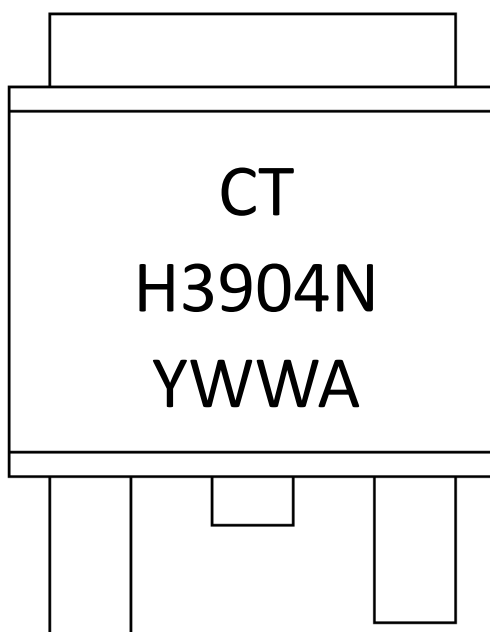
Recommended pad layout for surface mount leadform



Dimensions in mm unless otherwise stated



Marking Information



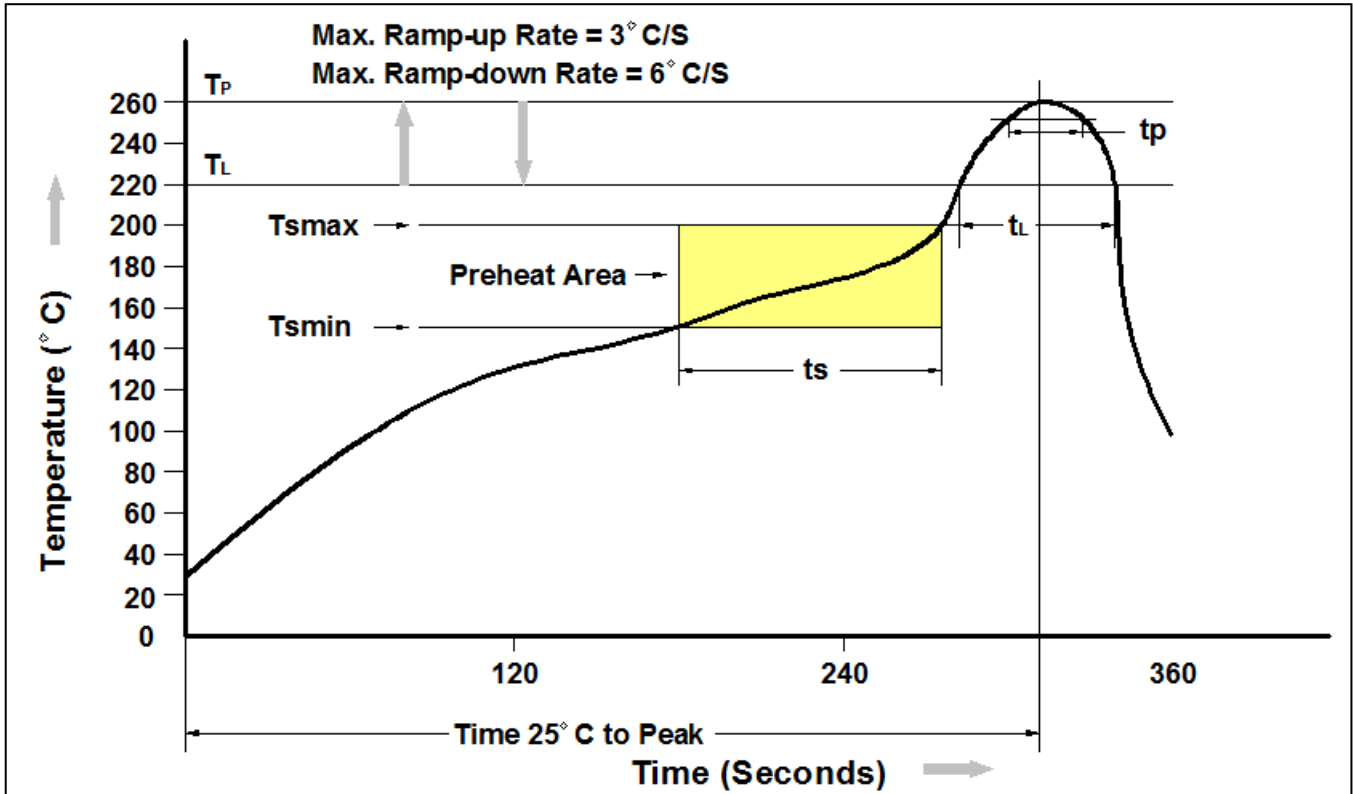
- CT : Denotes “ CT Micro”
- H3904N : Device Number
- Y : Fiscal Year
- WW : Work Week
- A : Production Code

Ordering Information

Part Number	Description	Quantity
CTH3904NS-T52	TO-252 Reel	2500 pcs



Reflow Profile



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (Tsmmin)	150°C
Temperature Max. (Tsmmax)	200°C
Time (ts) from (Tsmmin to Tsmmax)	60-120 seconds
Ramp-up Rate (tL to tp)	3°C/second max.
Liquidous Temperature (TL)	217°C
Time (tL) Maintained Above (TL)	60 – 150 seconds
Peak Body Package Temperature	260°C +0°C / -5°C
Time (tp) within 5°C of 260°C	30 seconds
Ramp-down Rate (TP to TL)	6°C/second max
Time 25°C to Peak Temperature	8 minutes max.



CTH3904NS-T52

N-Channel Enhancement MOSFET

DISCLAIMER

CT MICRO RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. CT MICRO DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

CT MICRO ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT EXPRESS WRITTEN APPROVAL OF CT MICRO INTERNATIONAL CORPORATION.

- 1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instruction for use provided in the labelling, can be reasonably expected to result in significant injury to the user.*
- 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.*